Evolution of Multithreaded Architectures Based on Dataflow

(Invited paper)

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Abstract

In this talk, we present an overview of the evolution of the multithreaded computer architectures. Future architectures of high performance systems will respond to forthcoming possibilities of technology and the increasing demand for attention to issues of programmability. Facing such challenges of high-performance computation, multithreaded processing element architectures represent a promising alternative to RISC architecture and its multiple-issue extension such as VLIW, superscalar, and superpipelined architectures.

The basic concepts and characteristics of multithreaded computer architectures are introduced. For multithreaded computer architecture, we keep two domains of application in mind: workstations and servers to support general purpose computation and massively parallel computers for scientific computation are covered. We describe several architectures representative of the design space for multithreaded, parallel computers based on dataflow models as case studies. We describe the design issues for multithreaded processing elements suitable for use as the node processor of parallel computers. These include the question of choosing appropriate program execution models, the organization of the processing element to achieve good utilization of major resources, the support for fine-grain interprocessor communication and global memory, and compiling machine code for multithreaded processors.

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